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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,073	01/23/2001	William Frederick Sauber	16356.573 (DC-02636)	2498
27683	7590	09/09/2005	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			NGUYEN, HAU H	
			ART UNIT	PAPER NUMBER
			2676	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/768,073	Applicant(s) SAUBER, WILLIAM FREDERICK	
	Examiner Hau H. Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 2-5, 7, 8, 11-14, 16, 17, 19 and 20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 6, 9, 10, 15, 18 and 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Arguments

1. Applicant's arguments filed June 20, 2005 have been fully considered but they are not persuasive.

In response to Applicant's arguments that reference Bickford et al. does not teach a switching device that is configured to receive video signals from a first video controller and a second video controller at respective inputs and to selectively provide such video signals to a compatible display device, the examiner disagrees. As cited in the previous Office Action, Bickford et al. teach a device 124 for selectively disabling either the video down AGP graphics accelerator 118 or the add-in AGP card seated 122 in the connector 120. Therefore, the output video signals from either of the video controllers is (selectively) received and forwarded to the display device via a connector, thus corresponding to the claimed switching device.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 6, 10, 15, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Bickford et al. (U.S. Patent No. 6,141,021).

Referring to claims 1; 6, 10, 15, and 21, as shown in Fig. 1 and described on page 1, lines 20-23, and page 2, lines 1-2 of the specification, admitted prior art teach a processor 110 is coupled to a chipset 120 that includes a bus input/output (I/O) controller 122, a memory

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controller 124, and an integrated video controller 126 (a first video controller). A system memory 130 is coupled to chipset 120. An optional video controller 140 (a second video controller) and a memory 142 are also included in computer system 100. Video controller 140 is coupled to chipset 120 using a port 144 such as an AGP port.

Thus, admitted prior art teach all the limitation of claims 1, 6, 10, 15, and 21, except for a switching device included in the chipset configured to receive video signals from either of the video controllers at respective inputs and provide the signals to a compatible display device.

However, as shown in Figs. 3 and 4, Bickford et al. teach an AGP video system 100, which is implemented on a system motherboard 130 (a chipset) (Fig. 4), comprising an AGP port 110. A location 116 is adapted to receive an AGP graphics accelerator chip 118 (a first video controller) and couple the graphics accelerator chip 118 to the AGP 110, thus providing an onboard, or video down AGP graphics accelerator. Further, a connector 120 (an interface coupled to the chipset) adapted to receive an AGP graphics accelerator add-in card 122 (a second video controller) is coupled to the AGP 110, along with a device 124 (a switching device) for selectively disabling either the video down AGP graphics accelerator 118 or the add-in AGP card seated 122 in the connector 120. Thus, two AGP graphics accelerators 118, 122 may be simultaneously coupled to the AGP 110, since the device 124 disables one of the AGP graphics accelerators 118, 122 and prevents both devices 118, 122 from contending for the AGP 110 (col. 4, lines 33-53). Bickford et al. further teach the switching device can be implemented using a pass-through switch to disable the video down AGP graphics accelerator chip when an add-in card is seated in the connector. The pass-through switch is arranged such that at least one signal is prevented from reaching the video down AGP graphics accelerator

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chip when it determines that an add-in card is seated in the connector, thereby disabling the video down AGP graphics accelerator chip. When the connector does not have an add-in card seated therein, it allows the signal to "pass-through" to the video down AGP graphics accelerator chip (Fig. 6, and col. 5, lines 66-67, and col. 6, lines 1-9). As shown in Figs. 1 and 2, the chipset is coupled to a system CPU 14 and system memory 18.

Therefore, it would have been obvious to one skilled in the art to utilize the switch device as taught by Bickford et al. in combination with the admitted prior art computer system in order to eliminate contention for an AGP among multiple AGP devices (col. 3, lines 32-33).

4. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Bickford et al. (U.S. Patent No. 6,141,021) further in view of Shin (U.S. Patent No. 6,804,724).

Referring to claims 9 and 18, as cited above, admitted prior art and Bickford et al. teach all the limitations of claims 9 and 18, except that the signals received by the switching device includes digital and analog signals.

However, Shin teaches a video card 520, as shown in Fig. 11, comprises a video controller 524, which can generate both analog and digital signals and provide these signals to an analog display device 100, and digital display device 600 via connectors 521 and 522 (col. 5, lines 39-61). As shown in Fig. 20, Shin further teaches the computer system 700 has a video output path control function (a switching device) that selectively determines the output path to the extra CRT monitor 100 or LCD monitor 600 in response to a video setup information stored in the system BIOS or special key input of the keyboard 770 (col. 10, lines 19-25).

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Since, as cited above, Bickford et al. teach a switching circuit coupled to receive video signals from one of the two video controllers (while disabling the other), Shin teaches a switching circuit that receive analog and digital signals and provide the signals to the compatible (analog or digital) display device, it would have been obvious to one skilled in the art to utilize the method as taught by Shin in combination with the method as taught in admitted prior art and Bickford et al. in order to provide for a maximum user convenience in connecting any of the digital display and analog display with one computer system since display adapter is capable of detecting monitor cable connection state, and also reduce the power consumption (col. 10, lines 64-67, and col. 11, lines 1-5).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778.

The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

H. Nguyen

09/01/2005



MATTHEW LUU
PRIMARY EXAMINER